

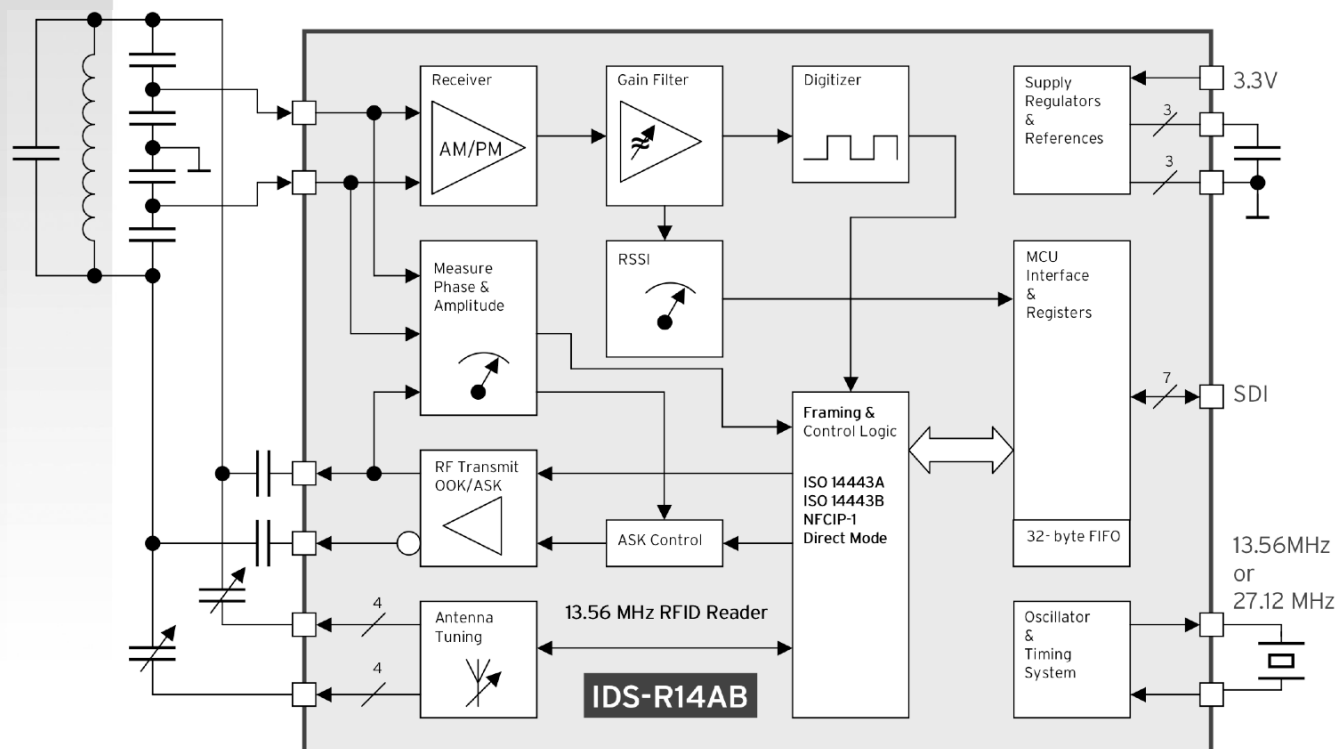
### Key Features

- Supply voltage range: 2.4V to 3.6V
- Automatic ASK modulation depth adjustment
- Extremely efficient for applications requiring low power consumption (@3.3V):
  - 25 mA for 40 mW output power
  - 16 mA for 15 mW output power
- High-resolution RSSI (8-bit A/D converter)
- Integrated supply regulators improving PSSR
- Integrated high-power output amplifier:
  - 400 mW with antenna tuning (@3.3V)
  - 800 mW without antenna tuning (@3.3V)
- Temperature range: -40°C to 85°C
- Low current consumption in NFC target mode: 3.5  $\mu$ A typical
- Supports Mifare® Ultralight 4-bit ACK/NACK reply

### Package Options

- 32-LD QFN (5x5 mm)

### Block Diagram



### Description

The IDS-R14AB is an integrated analogue front end and data framing system for ISO 14443A and B RFID systems. It also supports NFCIP-1 106-kbps active communication. Implementation of other standard and custom protocols is possible by only using AFE and implementing framing in external microcontroller (transparent mode).

The integrated serial peripheral interface (SPI) enables bi-directional communication with an external microcontroller. The IDS-R14AB performs all framing and synchronisation functions and hence a simple low cost microcontroller is sufficient to build a complete ISO 14443-compliant reader. It is intended for applications with direct antenna driver (no 50 $\Omega$  cable needed) and is especially suited for battery-powered readers requiring fast oscillator start-up time (~0.7 ms) and soft regulator start.

### Applications

- ISO 14443A/B RFID reader systems
- NFCIP-1 systems (NFC active communication)

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## 1 Related Documents

- Specification (Full Data Sheet): IDS-R14AB\_DS

## 2 Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	TIO	Digital I/O	Test IO pin
2	EN	Digital input with pull-down	Enable input
3	TEST	Digital input with pull-down	Test input
4	XTO	Analogue input	Xtal oscillator input
5	XTI	Analogue (digital) input	Xtal oscillator input (in test mode used as digital clock input)
6	VSN_D	Supply pad	Digital ground
7	VSP_A	Supply pad	Analogue supply regulator input
8	VDD	Supply pad	External positive supply
9	VSP_RF	Supply pad	Supply regulator output for antenna drivers
10	RFO1	Analogue output	Antenna driver output
11	RFO2	Analogue output	
12	VSN_RF	Supply pad	Ground of antenna drivers
13	TRIM1_3	Analogue input	Inputs for trimming antenna resonant circuit
14	TRIM2_3	Analogue input	
15	TRIM1_2	Analogue input	
16	TRIM2_2	Analogue input	
17	TRIM1_1	Analogue input	
18	TRIM2_1	Analogue input	
19	TRIM1_0	Analogue input	
20	TRIM2_0	Analogue input	
21	V <sub>SS</sub>	Supply pad	Ground, substrate of die
22	RFI1	Analogue input	Receiver Inputs
23	RFI2	Analogue input	
24	AGD	Analogue I/O	Analogue reference voltage
25	AD_IN	Analogue I/O Digital output	AD converter input, in analogue test modes used as analogue output, in logic test modes used as digital output
26	VSN_A	Supply pad	Analogue ground
27	INTR	Digital output	Interrupt request output
28	MCU_CLK	Digital output	Microcontroller clock output
29	SDATAO	Digital output with tristate	Serial Peripheral Interface data output
30	SDATAI	Digital input	Serial Peripheral Interface data input
31	SCLK	Digital input	Serial Peripheral Interface clock
32	SEN	Digital input	Serial Peripheral Interface data enable

### 3 Pin Configuration

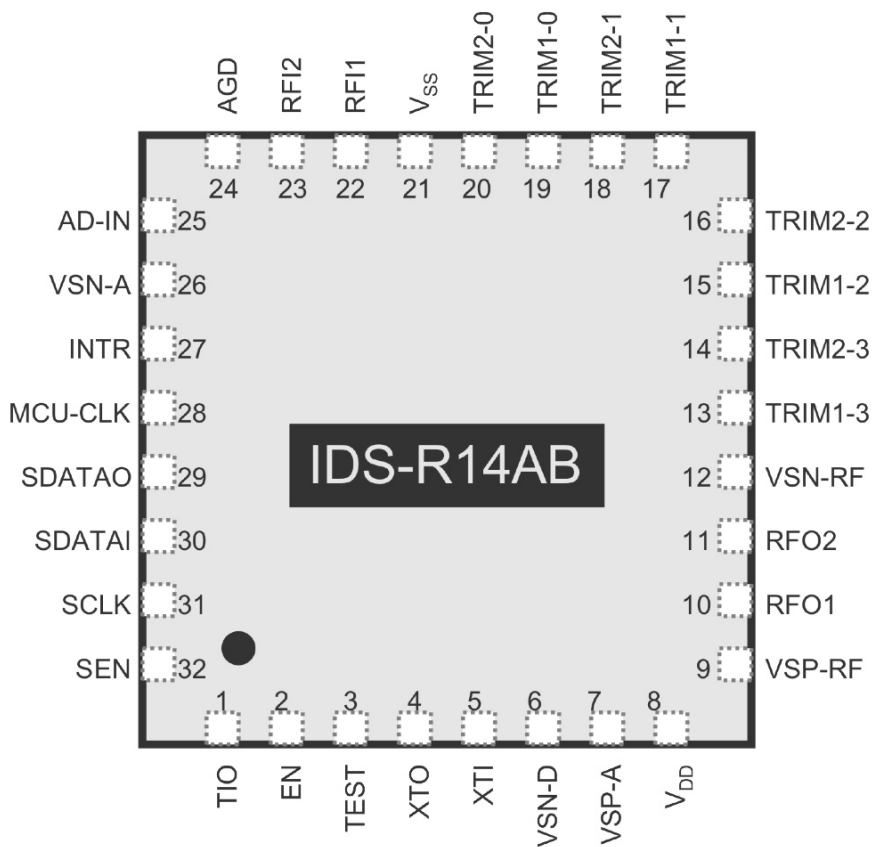


Figure 1: QFN 32 pinout (top view)

## 4 Absolute Maximum Ratings (Non-Operating)

(Operating free-air temperature range, unless otherwise noted)\*

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
DC supply voltage	$V_{DD}$	-0.5	5	V	
Input pin voltage (all except TRIM pins)	$V_{in}$	-0.5	5	V	
Input pin voltage TRIM pins	$V_{intrim}$	-0.5	30	V	
Input current (latchup immunity)	$I_{scr}$	-100	100	mA	Norm: Jedec 78
ESD	ESD	+/-2		kV	Norm: MIL 883 E method 3015 (Human Body Model)
Total power dissipation (all supplies and outputs)	$P_t$		<td>	mW	
Storage temperature	$T_{strg}$	-55	125	°C	
Package body temperature	$T_{body}$		260	°C	Norm: IPC/JEDEC J-STD-020C (note 1)
Humidity non-condensing		5	85	%	

\*Stresses beyond those listed under »Absolute Maximum Ratings« may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under »Operating Conditions« are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 1: The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices".

## 5 Operating Conditions

All in this specification defined tolerances for external components need to be assured over the whole operation conditions range and also over lifetime.

PARAMETER	SYMBOL	MIN	MAX	UNIT	REMARKS
Positive supply voltage	$V_{DD}$	2.4	3.6	V	Note 1
Negative supply voltage	$V_{SS}$	0	0	V	
Ambient temperature	$T_{amb}$	-40	85	°C	Note 2
Input pin voltage TRIM pins			30	V	

Note 1: In case power supply is lower than 2.6V, PSSR cannot be improved using internal regulators (minimum regulated voltage is 2.4V).

Note 2: The R14AB is designed to operate at temperatures up to 110°C. For operation at temperatures higher than 85°C, additional qualification is needed.

## 6 Application and System Description

### 6.1 System Diagram

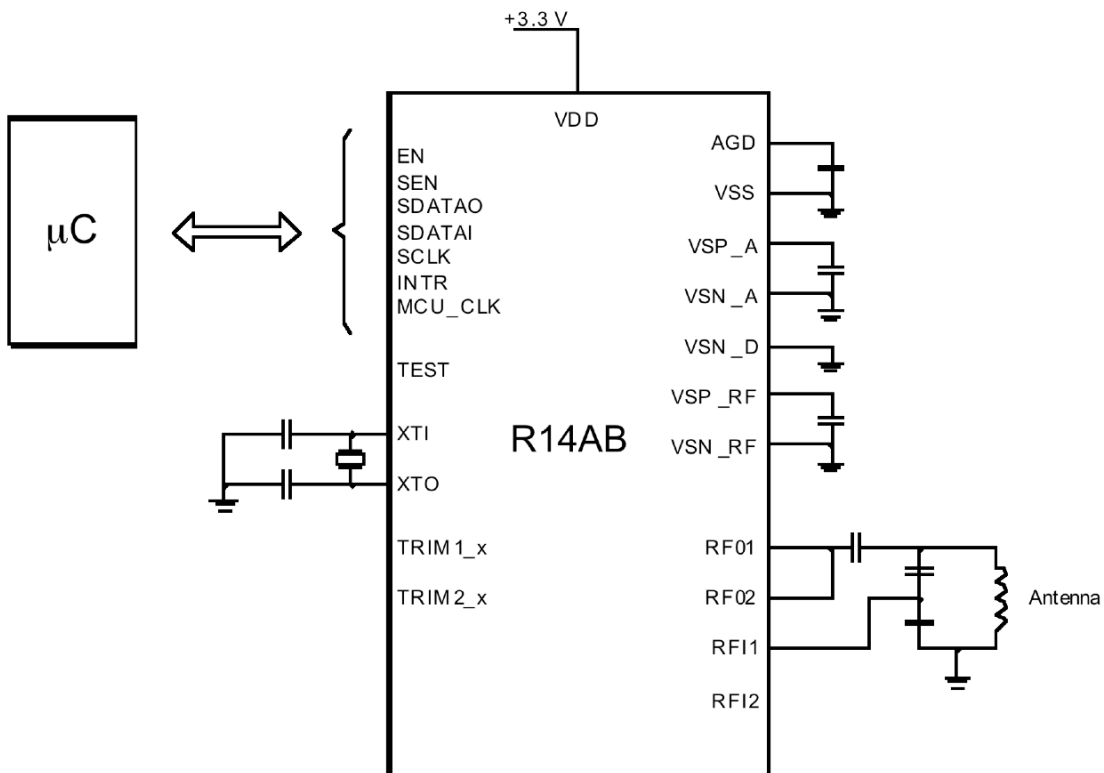


Figure 2: Minimum Configuration with Single-Sided Antenna Driver

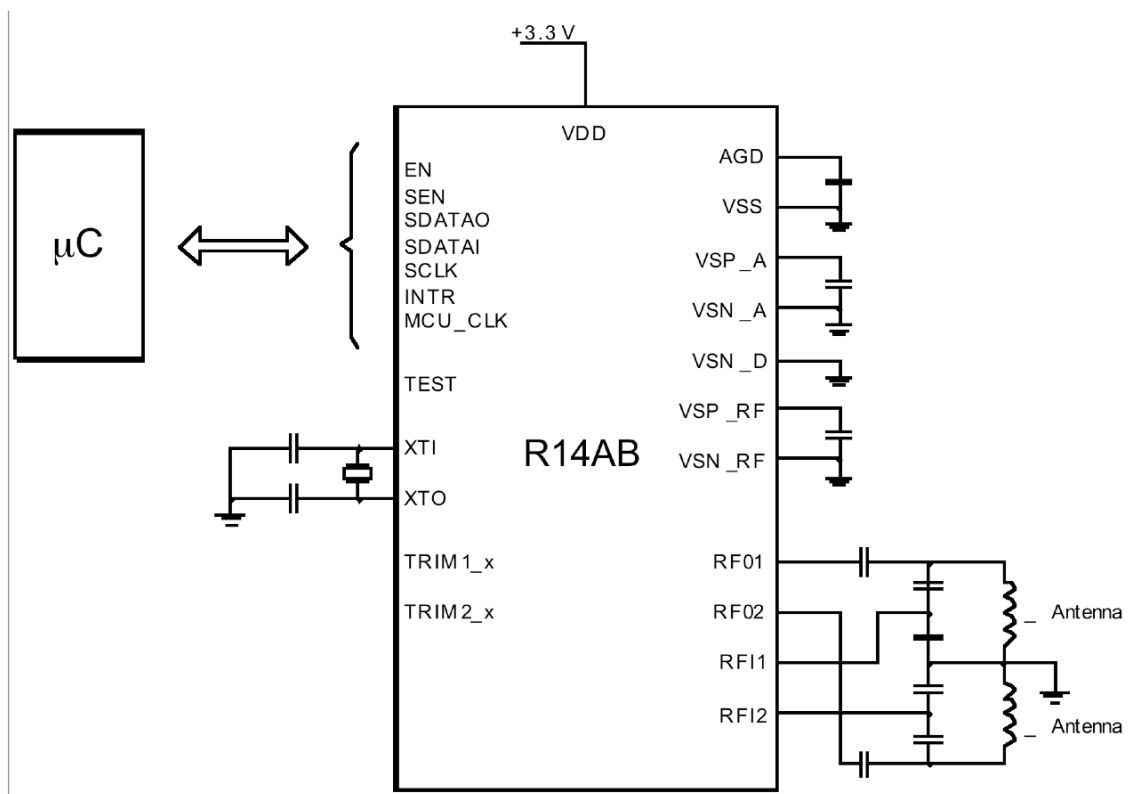


Figure 3: Minimum Configuration with Differential Antenna driver

## 6.2 Typical Applications

### 6.2.1 Minimum Configuration

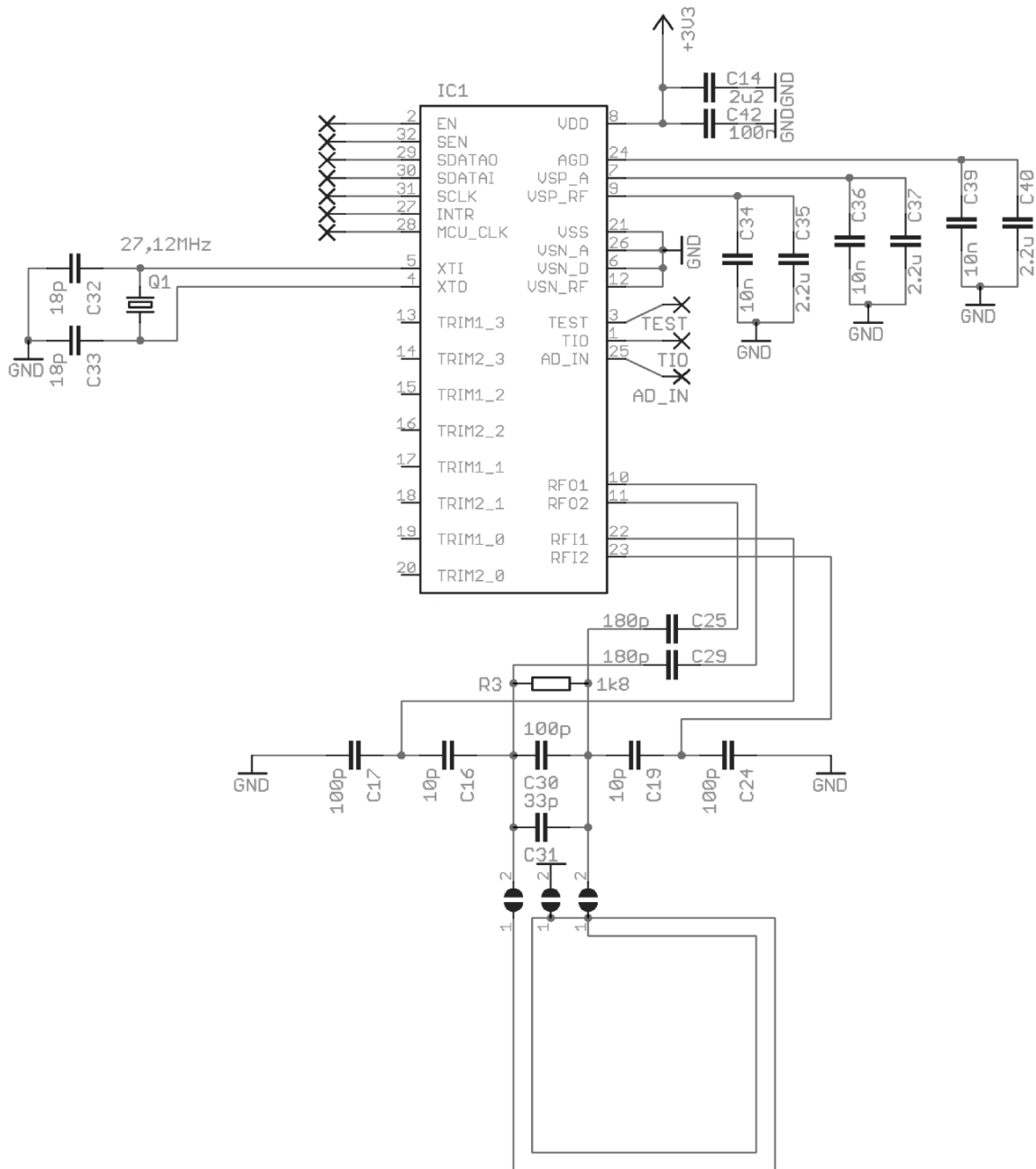


Figure 4: Typical Application with Minimum Configuration

### 6.2.2 Configuration with Antenna Trimming

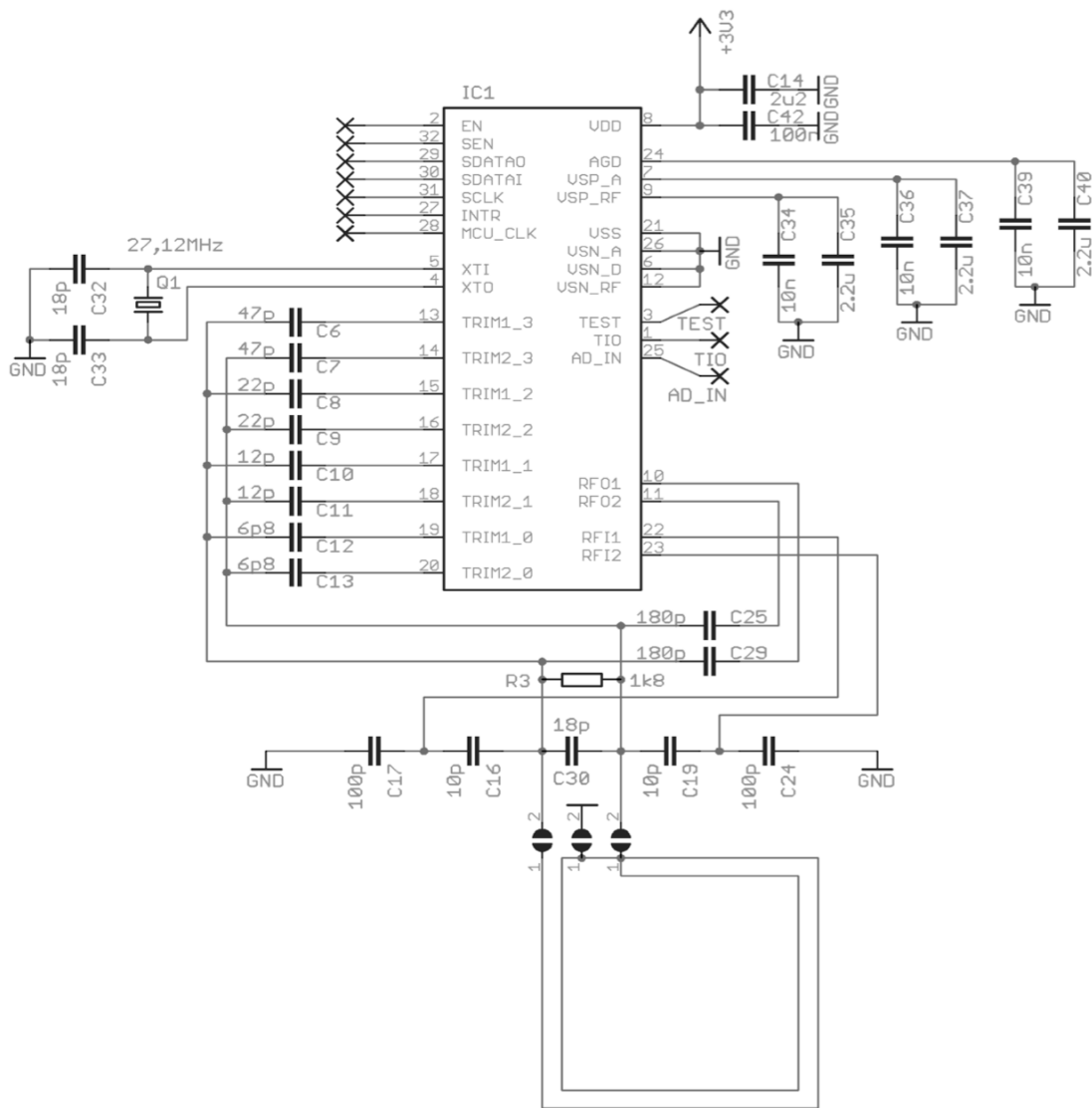


Figure 5: Typical Application with Antenna Trimming Capacitors

6.2.3 Configuration with Antenna Trimming and Output Filter

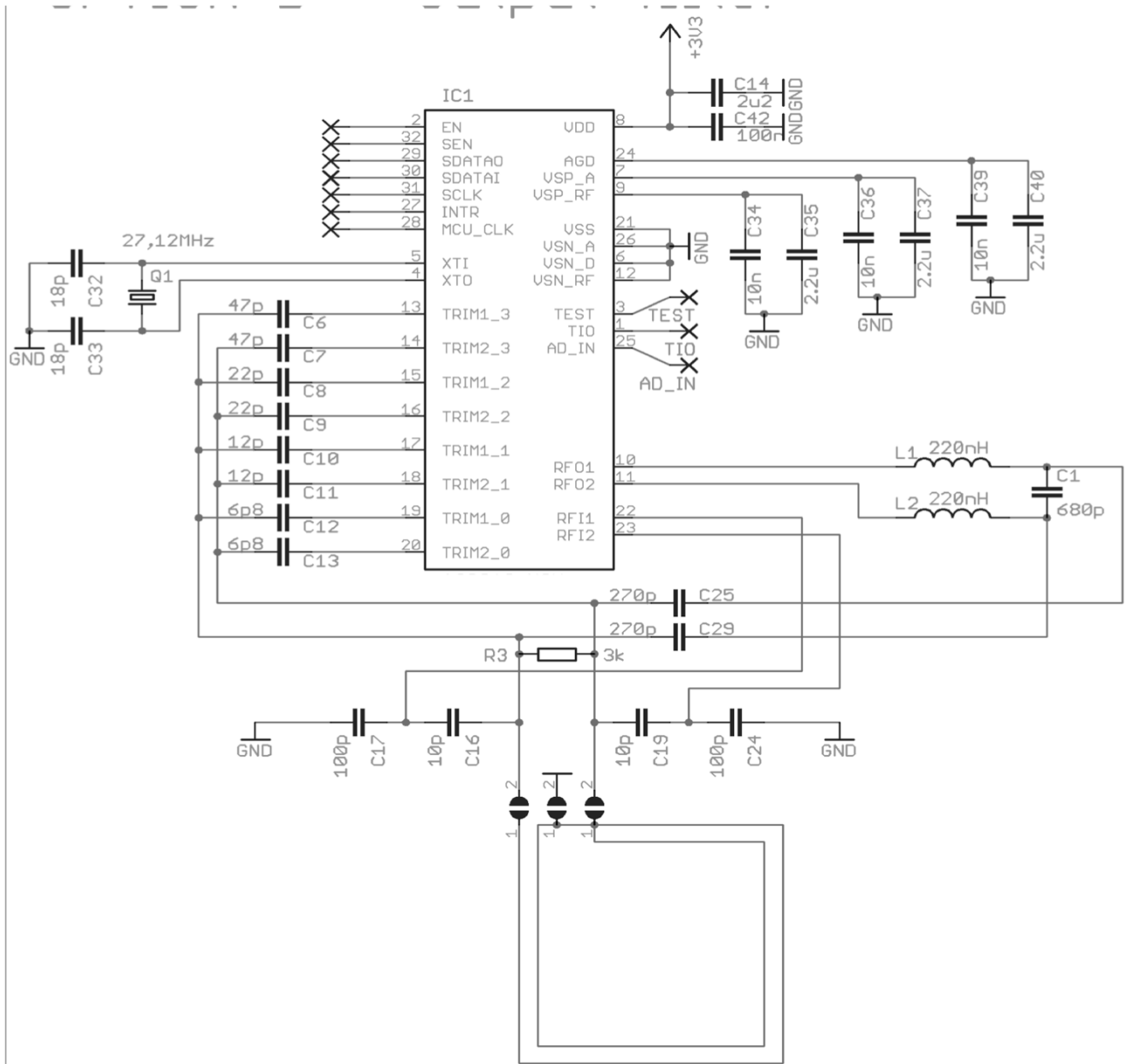


Figure 6: Typical Application with Antenna Trimming and Output Filter

### 6.3 Circuit Block Diagram

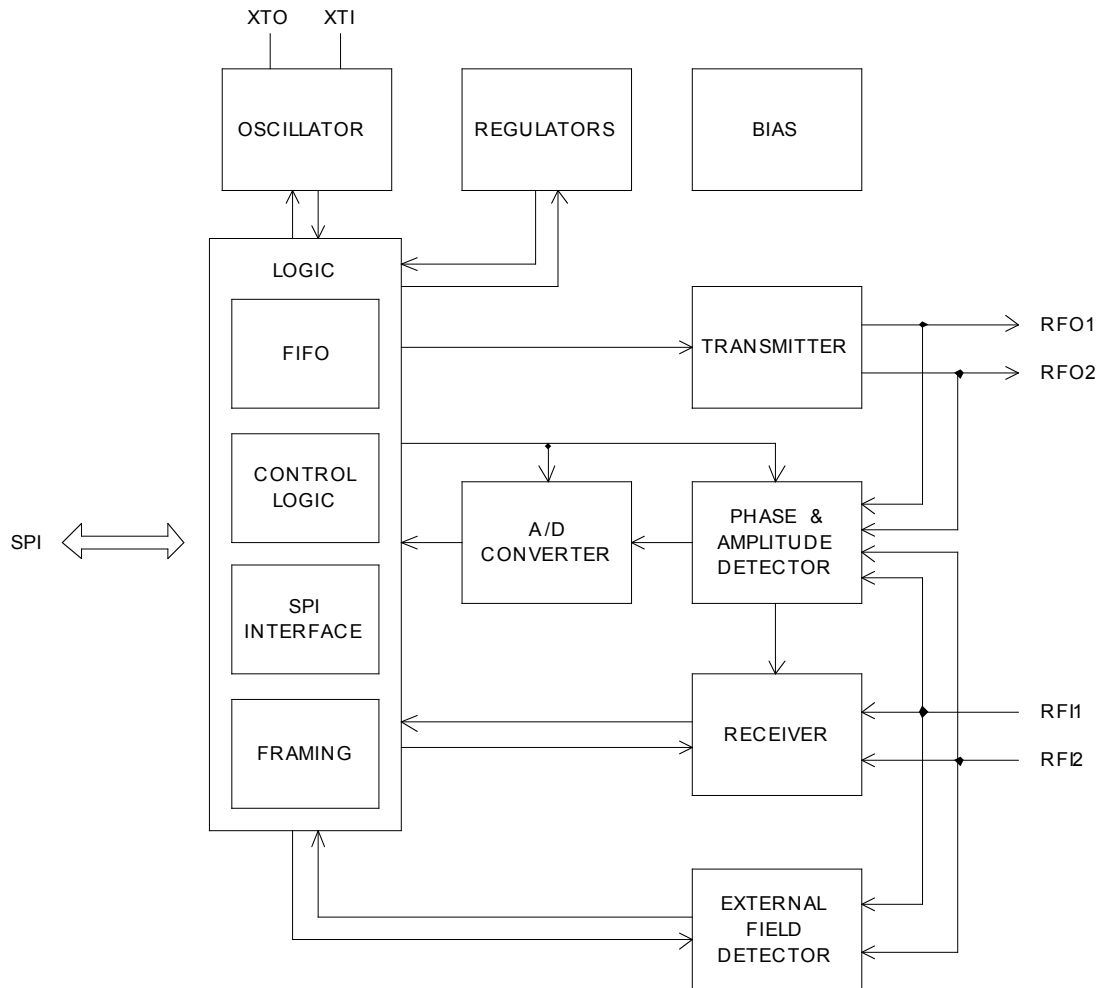


Figure 7: R14AB Building Blocks.

#### 6.3.1 Transmitter

Transmitter incorporates drivers, which drive external antenna through pads RFO1 and RFO2. Single sided and differential driving is possible. Transmitter block also contains circuits, which modulate transmitted signal for communication reader to transponder (OOK or configurable AM modulation).

##### 6.3.1.1 Close Loop Adjustment of AM Modulation Depth

Transmitter comprises a unique close loop adjustment of AM modulation depth (patent pending). Open loop adjustment of modulation depth (usually with some serial resistance) often results in modulation, which is either too deep or not deep enough. In first case supplying of ISO14443B tag during modulated periods might be problematic in second case modulation may not be detected. In case of close loop adjustments, a calibration procedure is performed (command

Calibrate Modulation Depth) during which modulation is observed through Receiver.

##### 6.3.1.2 Trimming of Antenna LC Tank

Transmitter also incorporates possibility of trimming of antenna LC tank resonant frequency (patent pending). This is done by connecting pads TRIM1x and TRIM2x to external binary weighted capacitors connected to antenna LC tank. Pads TRIM1x and TRIM2x contain switches. Command Calibrate Antenna starts a procedure during which external trim capacitors are connected to LC tank to reach optimal tuning. Optimal tuning is found by observing phase difference between transmitter output and receiver input. Phase detector block is used for that purpose.

R14AB transmitter is indented to directly drive antennas (without 50Ω cable, usually antenna is on the same PCB). Operation with 50Ω cable is also possible, but in that case some advanced features (LC tank tuning, <tbd>) are not possible. Please

note that transmitted power is lower in case of 50Ω cable system.

### 6.3.2 Receiver

Receiver detects tag modulation superimposed on 13.56MHz carrier signal. Receiver chain is composed of peak detector, two gain and filtering stages and digitizer stage. Filter characteristics are adjusted to optimize performance for different ISO modes and data rates (subcarrier frequencies from 212 kHz to 848 kHz are supported). Receiver chain inputs are pads RF11 and RF12, output of digitizer stage is demodulated subcarrier signal. Receiver also contains block which is detecting presence of external RF field in NFCIP target mode. Receiver chain incorporates several features, which enable reliable operation in different phase and noise conditions:

#### 6.3.2.1 AM and PM Demodulation with RSSI Measurement

AM or PM demodulation of receiving signal is possible to avoid having so called communications holes in reader operating volume. Choice between AM and PM demodulation is done by setting a bit in Configuration register 5 (#05); default setting is AM. While tag message is being processed by receiver an RSSI measurement is continually done and stored in peak-hold fashion in RSSI display register (#17). By comparing RSSI value in AM and PM mode external controller can decide for demodulation mode in which there is more signal. AM demodulation is done by processing peak detector signal, PM demodulation is done by processing phase signal coming from Phase detector.

#### 6.3.2.2 AGC and Gain Reduction

AGC (automatic gain control) feature is useful in case tag is close to the reader. In such conditions there is saturation in receiver chain in case gain is maximum and demodulation can be influenced by system noise and saturation of last gain stage. When AGC is switched on gain of last stage is reduced so that the input to digitiser stage is not saturated.

Receiver gain can also be reduced by setting appropriate bits in Receiver Control register.

#### 6.3.2.3 Squelch

This feature is designed to avoid demodulation problems of tags, which produce a lot of noise during data processing (while data sent by reader is processed and answer prepared). It can also be used in noisy environment. Tag processing noise (or environment noise) may be misinterpreted as start of tag response, which results in reader decoding error. These problems are avoided by reducing receiver gain so that there are no transitions of output when noise is present. This is

done by sending Squelch command while noise, which has to be eliminated, is present.

#### 6.3.2.4 RF Amplitude Measurement

Direct command Measure RF performs measurement of amplitude of signal present on RFI inputs and stores result in A/D register.

#### 6.3.2.5 Low Power Operation

Receiver has a low power mode in which its consumption is reduced from 10mA to 4mA. Of course in this mode also receiver sensitivity is reduced.

### 6.3.3 Phase Detector

Phase detector is observing phase difference between transmitter output signal and receiver input signal. Phase measurement is used for several purposes:

- Variation of signal phase are used to perform PM demodulation (already mentioned above)
- Antenna tuning and checking of antenna resonance.

Clock extracted from receiver input signal is also used to run self-mixer. Output of self mixer giving information about receiver input amplitude is fed to A/D converter. This information is available to user in DA register, it is also used internally for AM modulation depth adjustment.

### 6.3.4 A/D Converter

As already mentioned above R14AB contains a built in A/D Converter. Its input can be multiplexed from different sources and is used in several applications (measurement of RF amplitude, Calibrate Modulation Depth, Check Antenna Resonance, AD conversion of signal applied to input AD\_IN). Result of AD conversion is stored in a register which can be read through SPI interface.

### 6.3.5 External Field Detector

External field detector is a low power block, which is switched on in NFCIP target mode to detect presence of initiator field. It is also used during NFCIP Collision avoidance procedure.

### 6.3.6 Quartz Crystal Oscillator

Quartz crystal oscillator can operate with 13.56MHz and 27.12MHz crystals. At start-up the transconductance of oscillator is increased to achieve fast start-up. Since start-up time varies depending on crystal type, temperature and other parameters oscillator amplitude is observed and an interrupt is sent when stable operation is reached to inform controller that clock signal is stable and reader field can be switched on.

It also provides clock signal to external microcontroller (MCU\_CLK) according to setting in control register.

For better performance it is recommended to use 27.12MHz crystal. In case of using 27.12MHz crystal oscillator duty cycle of antenna driving signal is better controlled (it is internally divided).

### 6.3.7 Power Supply Regulators

Integrated power supply regulators ensure good power supply rejection of complete reader system. At power up regulators are transparent. In case PSRR of reader system has to be improved command Adjust regulators is sent. As result of this command power supply level of VDD is measured in maximum load conditions and regulated voltage reference is set 200 mV below this measured level to assure stable regulated supply. Resulting regulated voltage is stored in a register. It is also possible to define regulated voltage by writing a configuration register. In order to decouple noise sources from different parts of IC there are two regulators integrated with separated external blocking capacitors (regulated voltage of both is the same). One regulator is for analog blocks, the other one for antenna drivers. Logic and digital I/O pads are supplied directly from VDD (VSS pin for logic and digital I/O is separated to avoid coupling of logic induced noise in substrate).

Additionally to power supply regulators there is a separate subblock which generates reference voltage for analog processing (AGD - analog ground). This voltage also has an associated external buffer capacitor.

### 6.3.8 POR and Bias

This block contains bias current and voltage generator, which provide bias currents and reference voltages to all other blocks. It also incorporates Power on Reset (POR) subblock

which provides reset at power-up and at low supply levels.

### 6.3.9 ISO14443 and NFCIP Framing

This block performs ISO14443 and NFCIP-1 106 kbps active communication framing for receive and transmit according to mode and data rate settings.

In receive it takes demodulated subcarrier signal from Receiver. It recognises SOF, EOF and data bits, performs parity and CRC check, organises received data in bytes and places them in FIFO.

During transmit it performs inversed operations, it takes bytes from FIFO, generates parity and CRC bits, adds SOF and EOF and performs final encoding before passing modulation signal to transmitter.

In Transparent mode framing and FIFO are bypassed, demodulated signal from Receiver is directly sent to SDATAO pin, signal applied to SDATAI pin is directly used to modulate transmitter.

### 6.3.10 FIFO

R14AB contains a 32-byte FIFO. Depending on mode it contains either data, which has been received or data, which is to be transmitted.

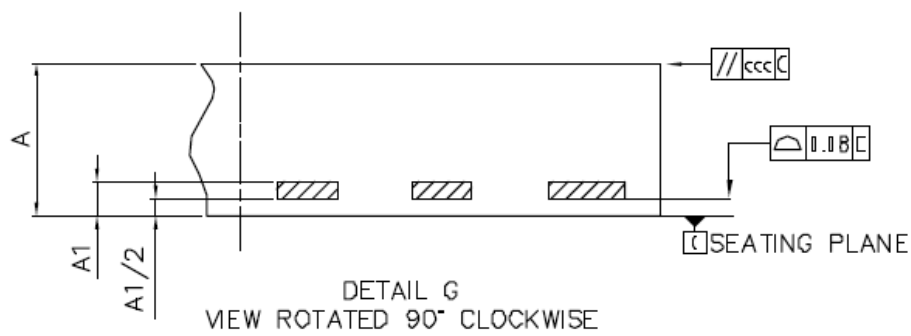
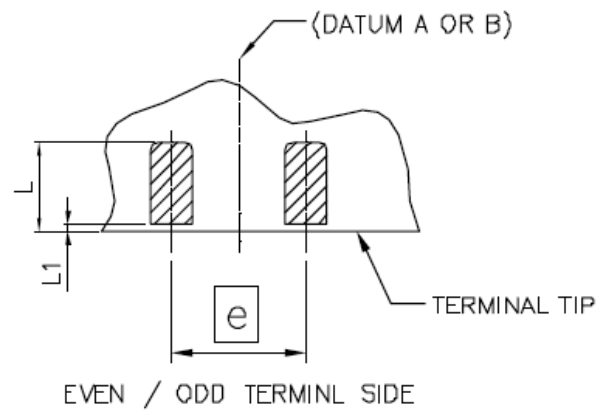
### 6.3.11 Control Logic

Control logic contains I/O registers, which define operation of device.

### 6.3.12 SPI Interface

Serial Peripheral interface (SPI) is used for communication between external microcontroller and R14AB.





DIM	MIN	NOM	MAX	NOTES
A	0.80	0.90	1.00	1. Dimensioning and tolerancing confirm to ASME Y14.5M-1994. 2. All dimensions are in millimeters. Angles are in degrees. 3. Dimension b applies to metallized terminal and is measured between 0.25mm and 0.30mm from terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1mm is acceptable. 4. Coplanarity applies to the exposed heat slug as well as the terminal. 5. Radius on terminal is optional.
A1	0.203 REF			
b	0.33	0.40	0.47	
D	5.00 BSC			
E	5.00 BSC			
D1	3.15	3.25	3.35	
E1	3.15	3.25	3.35	
e	-	0.80 BSC	-	
L	0.255	0.355	0.455	
L1			0.10	
P	45° BSC			
aaa		0.10		
ccc		0.10		

The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices".

## 8 Ordering Information

ORDERING CODE	DESCRIPTION	OPERATING TEMPERATURE RANGE	PACKAGE TYPE	DEVICE MARKING	SHIPPING FORM
R14AB/QFN32/T&R	ISO 14443A/B HF Reader IC	-40°C to 85°C	32-LD QFN (5x5 mm) RoHS*	R14AB	Tape & Reel 1000 parts/reel

\*) Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

Order quantities should be a multiple of shipping form.

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