

Key Features

- Supply voltage range 4.1 to 5.5V
- Protocol: ISO 18000-6C / EPC Gen2 (full protocol support) and ISO 18000-6A/B (in direct mode)
- Filters dedicated to 250kHz and 320kHz M4 and M8 DRM operation
- Antenna driver using ASK or PR-ASK modulation
- AM & PM demodulation eliminating communication holes through automatic I/Q selection
- 3.3V voltage regulator providing up to 20 mA for external MCU
- On-board VCO and PLL covering complete RFID frequency range from 840MHz to 960MHz
- Significant increase of PSRR through on-chip RF output supply regulators
- Power-down, standby and active mode
- Can be USB powered
- Supports frequency hopping
- Selectable clock output for MCU

Description

The R902DRM UHF reader chip is an integrated analogue front end and protocol handling system for a 900MHz RFID reader system. Built in programming options make it suitable for a wide range of UHF RFID applications. The R902DRM offers functionality of the R901G chip and is dedicated to operation on the DRM link frequencies used in ETSI and FCC regions.

The reader configuration is achieved by selecting the desired protocol settings in the control registers. Direct access to all control registers also allows fine-tuning of different reader parameters.

The R902DRM complies with EPC Class 1 Generation 2 protocol (ISO 18000-6C) and ISO 18000-6A/B (in direct mode).

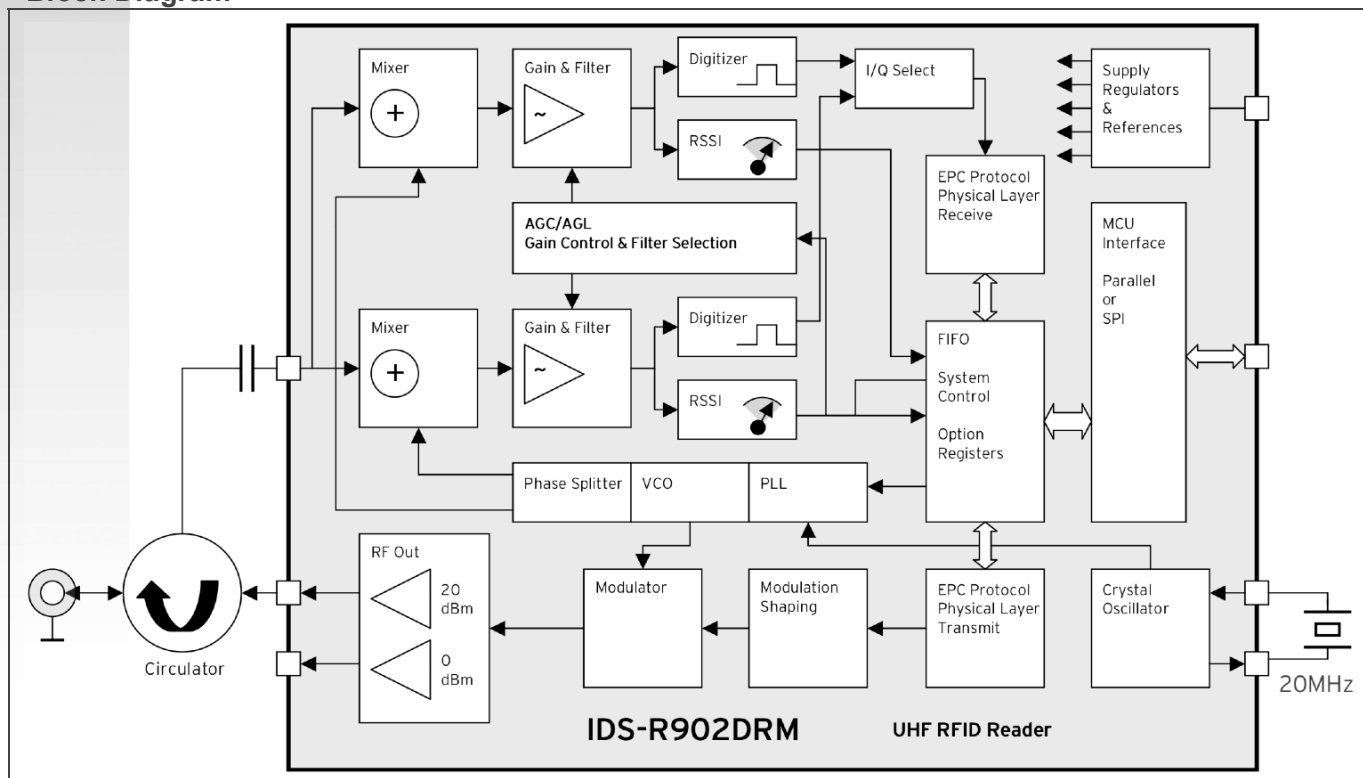
Applications

- UHF RFID reader systems
- Hand-held UHF RFID readers

Package

64-LD QFN (9 x 9 mm)

Block Diagram



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3 Related Documents

Specification (full data sheet): R902DRM_DS

Key Characteristics and Benefits

- ISO18000-6C (EPC Gen2) full protocol support
- ISO18000-6A/B compatibility in direct mode
- Filters dedicated to 250kHz and 320kHz M4 and M8 DRM operation
- Available RX modes:
LF40kHz, 160kHz: FM0, M2, M4, M8
LF 250kHz, 320kHz, 640kHz: M4, M8
- Integrated low level transmission coding
- Integrated low level decoders
- Integrated data framing
- Integrated CRC checking
- Parallel 8 bit or serial 4 pin SPI interface to MCU using a 24 bytes FIFO
- Voltage range for communication to MCU between 1.8V and 5.5V
- Selectable clock output for MCU
- Integrated supply voltage regulator (20 mA) which can be used to supply MCU and other external circuitry
- Integrated supply voltage regulator for the RF output stage, providing rejection to supply noise
- Internal power amplifier (20dBm) for short-range applications.
- Modulator using ASK or PR-ASK modulation
- Adjustable ASK modulation index
- AM & PM demodulation ensuring no “communication holes” with automatic I/Q selection
- Built in reception low-pass and high-pass filters having selectable corner frequencies.
- Selectable reception gain
- Reception automatic gain control
- A/D converter for measuring TX power using external RF power detector

- D/A converter for controlling external power amplifier
- Frequency hopping support
- On-board VCO and PLL covering complete RFID frequency range 840MHz to 960MHz
- Oscillator using 20MHz crystal
- Power down, standby and active mode
- Can be USB powered

5 Pin Configuration

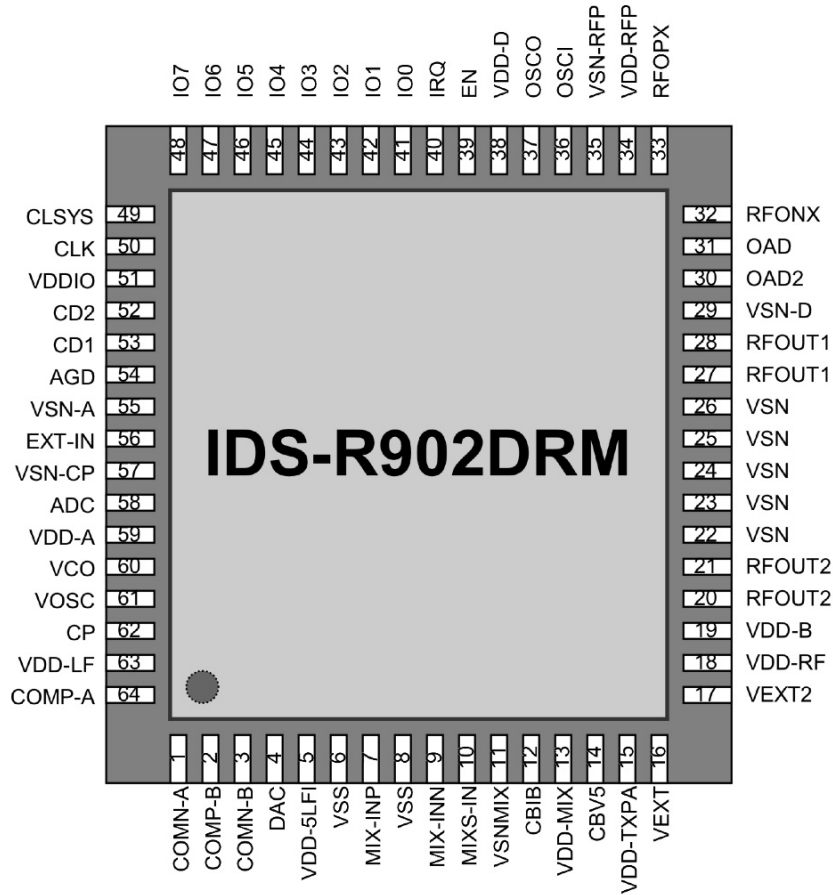


Figure 1: Pin Configuration for 64-LD QFN

6 Pin Description

PIN	IDS-R902DRM	TYPE	DESCRIPTION
1	COMN_A	BID	Internal node, connect de-coupling capacitor to VDD_5LFI
2	COMP_B	BID	Internal node, connect de-coupling capacitor to VDD_5LFI
3	COMN_B	BID	Internal node, connect de-coupling capacitor to VDD_5LFI
4	DAC	OUT	DAC output for external amplifier support
5	VDD_5LFI	SUP	Positive supply for LF input stage, connect to VDD_MIX
6	VSS	SUP	Substrate
7	MIX_INP	INP	Differential mixer positive input
8	VSS	SUP	Substrate
9	MIX_INN	INP	Differential mixer negative input
10	MIXS_IN	INP	Single ended mixer input
11	VSN_MIX	SUP	Mixer negative supply
12	CBIB	BID	Internal node de-coupling capacitor to ground
13	VDD_MIX	SUP	Mixer positive supply, internally regulated to 4.8V
14	CBV5	BID	Internal node de-coupling capacitor to VDD_MIX
15	VDD_TXPAB	SUP	Bias positive supply. Connect to VDD_MIX.
16	VEXT	SUP	Main positive supply input (5...5.5V)
17	VEXT2	SUP	PA positive supply regulator input (2.5... 5.5V)
18	VDD_RF	SUP	PA positive supply regulator output, internally regulated to 2...3.5V
19	VDD_B	SUP	PA buffer positive supply. Internally regulated to 3.4V
20	RFOUT2	OUT	PA positive RF output
21	RFOUT2	OUT	PA positive RF output
22	VSN	SUP	PA negative supply
23	VSN	SUP	PA negative supply
24	VSN	SUP	PA negative supply
25	VSN	SUP	PA negative supply
26	VSN	SUP	PA negative supply
27	RFOUT1	OUT	PA negative RF output
28	RFOUT1	OUT	PA negative RF output
29	VSN_D	SUP	Digital negative supply
30	OAD2	BID	Analogue or digital received signal output and MCU support mode sense input
31	OAD	BID	Analogue or digital received signal output
32	RFONX	OUT	Low power linear negative RF output (~0dBm)
33	RFOPX	OUT	Low power linear positive RF output (~0dBm)
34	VDD_RFP	SUP	RF path positive supply, internally regulated to 3.4V
35	VSN_RFP	SUP	RF path negative supply
36	OSCI	INP	Crystal oscillator input
37	OSCO	BID	Crystal oscillator output or external 20MHz clock input
38	VDD_D	SUP	Digital part positive supply, internally regulated to 3.4V
39	EN	INP	Enable input
40	IRQ	OUT	Interrupt output
41	IO0	BID	I/O pin for parallel communication
42	IO1	BID	I/O pin for parallel communication
43	IO2	BID	I/O pin for parallel communication. Enable RX input in case of direct mode
44	IO3	BID	I/O pin for parallel communication Modulation input in case of direct mode
45	IO4	BID	I/O pin for parallel communication Slave select in case of serial communication (SPI)
46	IO5	BID	I/O pin for parallel communication SCLK clock in case of serial communication (SPI) Sub-carrier out or bit clock output in case of direct mode
47	IO6	BID	I/O pin for parallel communication. MISO in case of serial communication (SPI) Sub-carrier out or data output in case of direct mode
48	IO7	BID	I/O pin for parallel communication. MOSI in case of serial communication (SPI)
49	CLSYS	OUT	Clock output for MCU operation
50	CLK	INP	Clock input for MCU communication (parallel and serial)
51	VDD_IO	SUP	Positive supply for peripheral communication, connect to host positive supply
52	CD2	BID	Internal node de-coupling capacitor
53	CD1	BID	Internal node de-coupling capacitor
54	AGD	BID	Analogue reference voltage
55	VSN_A	SUP	Analogue part negative supply
56	EXT_IN	INP	RF input in case external VCO is used
57	VSN_CP	SUP	Charge pump negative supply
58	ADC	IN	ADC input for external power detector support
59	VDD_A	SUP	Analogue part positive supply, internally regulated to 3.4V
60	VCO	INP	VCO input
61	VOOSC	BID	Internal node de-coupling capacitor
62	CP	OUT	Charge pump output
63	VDDLf	SUP	Positive supply for LF processing, internally regulated to 3.4
64	COMP_A	BID	Internal node, connect de-coupling capacitor to VDD_5LFI

7 Short Description

The R902DRM UHF reader chip is integrated analogue front end and protocol handling system for a 900MHz RFID reader system. Built in programming options make it suitable for a wide range of UHF RFID applications. The R902DRM offers functionality of the previous R901G chip and is dedicated to operation on the DRM link frequencies used in ETSI and FCC region.

The reader configuration is achieved by selecting the desired protocol in control registers. Direct access to all control registers also allows fine-tuning of different reader parameters.

Parallel or serial interface can be selected for communication between the host system (MCU) and the reader IC. When hardware coders and decoders are used for transmission and reception, the data is transferred via a 24-bytes FIFO register. In case of direct transmission or reception coders and decoders are bypassed and the host system can service the analogue front end in real time.

The transmitter generates 0dBm or 20dBm output power into 50Ω load and is capable of ASK or PR-ASK modulation. The integrated supply voltage regulators ensure supply rejection of the complete reader system.

The transmission system comprises low-level data coding. Automatic generation of FrameSync, Preamble, and CRC is supported.

The receiver system allows AM and PM demodulation. The receiver also comprises automatic gain control option (patent pending) and selectable gain and signal bandwidth to cover a range of input link frequency and bit rate options. The signal strength of AM and PM modulation is measured and can be accessed in RSSI register. The receiver output is selectable between digitized sub-carrier signal and output of one of the integrated sub-carrier decoders. The selected decoder delivers bit stream and data clock as outputs.

The receiver system comprises framing system. It performs the CRC check and organizes the data in bytes. Framed data is accessible to the host system through a 24-byte FIFO register.

To support external MCU and other circuitry a 3.3V regulated supply and clock outputs are available. The regulated supply has 20mA current capability.

8 Absolute Maximum Ratings

Operating free-air temperature range, unless otherwise noted

Supply Voltage Range V_{EXT} and V_{EXT2} (Note 3)	-0.3 V to 6 V
Maximum Positive Voltage – Pins:	
EN, IO7..IO0, CLK, IRQ, CLSYS, VDDIO, VDD_MIX, VDD_5LFI, VDD_TXPAB, CBV5, DAC, OAD, OAD2	$V_{EXT} + 0.3V$
Positive Voltage - Other Pins	4.5V
Maximum Negative Voltage - Other Pads	-0.3V
Latch-up immunity, according to JEDEC 78 (Note 4) I_O	± 100 mA
ESD Rating, according to MIL 883E method 3015	
RF pins, HBM	1 kV
Other pins, HBM	2 kV

Maximum Operating Virtual Junction Temperature (Note 2) T_J	120°C
Maximum Lead Temperature, 1.6 mm from case for 10 sec. (IPC/JEDEC J-STD-020C)	260°C
Storage Temperature, T_{stg}	-55°C to +150°C

Note 1: The absolute maximum ratings under any condition are limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified are not implied.

Note 2: The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

Note 3: All voltage values are with respect to substrate ground terminal V_{SS} .

Note 4: The AGD pin is excluded from the Latch-up immunity test at EN pin high. AGD is a reference voltage pin and must be kept at the reference voltage level for correct operation. AGD must be connected to external capacitor.

8.1 Electrical Discharge Sensitivity

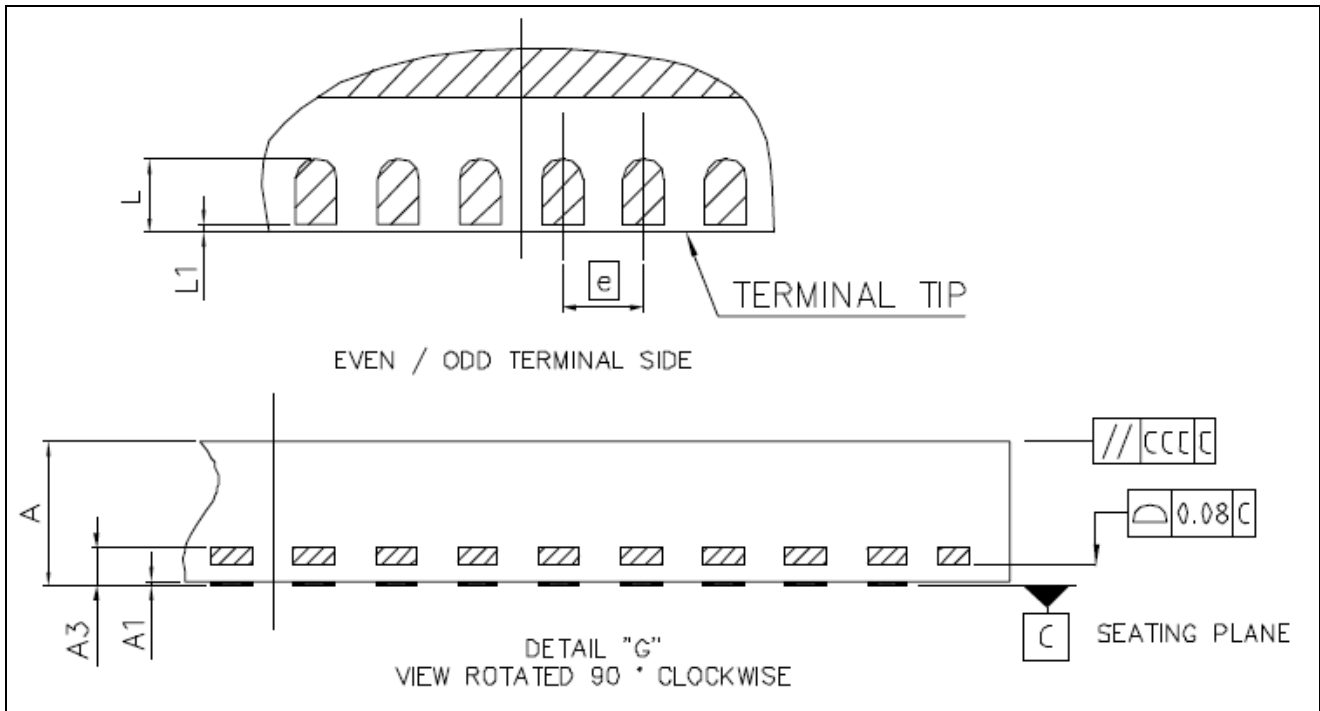
This integrated circuit can be damaged by ESD. We recommend that all integrated circuits are handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet the published specifications. RF integrated circuits are also more susceptible to damage due to use of smaller protection devices on the RF pins, which are needed for low capacitive load on these pins.

9 Operating Conditions

(Operating free-air temperature range)

Positive Supply Voltage, V_{EXT}	5.0V to 5.5V; typical 5.3V
Positive Supply Voltage, V_{EXT} ; bit vext_low = 1	4.1V to 5.5V
Operating virtual junction temperature range, T_J	-40°C to +110°C
Maximum operating temperature range	-40°C to +110°C



DIM	MIN	NOM	MAX	NOTES
A	0.80	0.85	0.90	1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
A1	0.00		0.05	
A3		0.203 REF		2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
b	0.20	0.25	0.30	
D		9.00 BSC		3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.
E		9.00 BSC		
D2	7.24	7.34	7.44	4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
E2	7.24	7.34	7.44	
e		0.50 BSC	-	5.0 RADIUS ON TERMINAL IS OPTIONAL.
L	0.40	0.45	0.50	
L1			0.10	
L2	0.35	0.40	0.45	
P		45° BSC		
aaa		0.15		
ccc		0.10		

11 Ordering Information

ORDERING CODE	DESCRIPTION	OPERATING TEMPERATURE RANGE	PACKAGE TYPE	DEVICE MARKING	SHIPPING FORM
R902DRM	UHF RFID Reader IC EPC Class 1 Gen2 (ISO 18000-6C)	-40°C to 110°C	QFN 64 (9 x 9 mm) RoHS*	IDS R902DRM	50 parts/reel

*) Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

Order quantities should be a multiple of shipping form.

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